REMARKS

Claims 5-11 and 15-25 were previously pending, of which claim 23 has been amended, claims 5, 6, 8-11, 15, 18-22, 24 and 25 remain in their original form, except for removal of reference letters "a", "b", and so forth, and claims 7, 16 and 17 were previously presented. Applicants note with appreciation the allowance claims 7-11, 16 and 17. Reconsideration of presently pending claims 5-11 and 15-25 is respectfully requested in light of the above amendments and the following remarks.

Claim Objections

Claim 23 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Claim 23 has been rewritten in independent form and is in condition for allowance.

Rejections Under 35 U.S.C. §103

Claims 5, 6, 15, 20-22 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Pfiester (US Patent No. 5,021,354 hereinafter referred to as "Pfiester") in view of Ahn (US Patent No. 5,874,330 hereinafter referred to as "Ahn"). Applicant traverses this rejection on the grounds that these references are defective in establishing a prima facie case of obviousness with respect to claims 5, 6, 15, 20-22 and 25. It is submitted that, in the present case, the Examiner has not factually supported a *prima facie* case of obviousness for the following, mutually exclusive, reasons.

Claim 5

Claim 5 recites:

5. A method of forming multiple spacer widths on a substrate, comprising:

providing a substrate with isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions;

forming a first gate electrode on said dielectric layer in said first transistor region, a second gate electrode on said dielectric layer in said second transistor region, and a third gate electrode on said dielectric layer in said third transistor region, said first gate electrode having a greater thickness than said second gate electrode and said second gate electrode having a greater thickness than said third gate electrode;

forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions; and

etching said oxide layer to form spacers with a first width adjacent to said first gate electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode.

1. The References Are Not Properly Combinable if Their Intended Function is Destroyed

It is clear that the Pfiester and Ahn patents are not properly combinable since, if combined, their intended function is destroyed. More particularly, Pfiester discloses using a sidewall spacer forming material which is selectively etchable with respect to the silicon dioxide upon which the spacer material is deposited, such as silicon nitride. (See Pfiester, col. 4, lines 56-61). Because of the height of the gate structure and the nature of the anisotropic etch process, two different spacer widths are formed from the silicon nitride layer that was deposited over the oxide layer. (See Pfiester, col. 4, lines 64-68; col. 5, lines 1-12).

Ahn discloses a transistor structure with different spacer widths for peripheral (logic) circuits than for cell (memory) circuits. However, Ahn accomplishes this by using nitride spacers for transistors in the cell region and in a separate process step by using oxide spacers for transistors in the peripheral region. This is because using identical nitride spacers for transistors in the cell region as well as transistors in the peripheral region has caused problems such as "increas[ing] an overlap capacitance of the gate-source electrodes, and caus[ing] an adverse effect on the device due to an increase in hot carrier generation." (See Ahn, col. 1, lines 41-49). In addition, the silicon nitride sidewall spacer in the cell (memory) region is necessary because

nitride has a better selectivity than oxide to secure an adequate process for contact etching for the bit line of the memory circuit. (See Ahn, col. 2, lines 11-18). Thus, it is clear that Ahn's device employs nitride spacers in the cell region and oxide spacers in the peripheral region in order to have optimal performance.

As stated in the Office Action, "it would have been obvious to a person having skill in the art to augment Pfiester's transistor structure...such as suggested by the combination of Pfiester's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer thicknesses, in order to form both CMOS transistors of both logic and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance." Applicants respectfully traverse the assertion that it would have been obvious to augment Pfiester's transistor structure with the teachings of Ahn in this manner.

As discussed above, augmenting Pfiester's transistor structure comprising silicon nitride spacers for both NMOS and PMOS transistors with Ahn's teaching of using nitride spacers for transistors in the cell region and in a separate process step of using oxide spacers for transistors in the peripheral region is inconsistent with the teachings and is not obvious. Moreover, Ahn's device employs nitride spacers with the same thickness for the transistors in the cell (memory) region because these transistors are of the same type and perform the same function—each transistor (along with a capacitor) stores 1 bit of data. (See Ahn, Figs. 2a-2g).

Since this modification of the Ahn patent clearly destroys the purpose or function of the invention disclosed in the patent, one of ordinary skill in the art would not have found a reason to make the claimed modification. Thus, for this mutually exclusive reason, the examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

2. Prior Art That Teaches Away From the Claimed Invention Cannot be Used to Establish Obviousness

In the present case the Ahn reference, by providing different spacer widths as a result of using two different materials and two separate etch steps, silicon nitride spacers for transistors in the cell region and oxide spacers for transistors in the peripheral region, clearly teaches away from claim 5. Claim 5 recites in part "(c) forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions; and (d) etching said oxide layer to form spacers with a first width adjacent to said first gate electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode." Applicants submit that the Ahn reference teaches away from etching a single oxide layer to create spacers of different widths.

MPEP § 2142.02 requires that "[a] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." Thus, for this reason alone, the examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

3. Even When Combined, the References Do Not Teach the Claimed Subject Matter

As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness,...the prior art reference (or references when combined) must teach or suggest all the claim limitations." As stated in the Office Action, Pfiester discloses only two different spacer widths and fails to disclose any additional widths. Ahn discloses only two different spacer widths, one for the peripheral region and the other for the cell region. However, Ahn accomplishes this difference by using two separate layers of material and two separate etch procedures. In contrast, claim 5 discloses a method of forming three different spacer widths by "(c) forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions; and (d) etching said oxide layer to form spacers with a first width adjacent to said first gate electrode,

spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode." Therefore, even when combined, the references of record do not teach or suggest all the limitations recited in claim 5.

Thus, for this mutually exclusive reason, the examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

4. The Combination of References is Improper

Assuming, arguendo, that none of the above arguments for non-obviousness apply (which is clearly not the case based on the above), there is still another, mutually exclusive, and compelling reason why the Pfiester and Ahn patents cannot be applied to reject claim 5 under 35 U.S.C. § 103.

§ 2142 of the MPEP also provides, "the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made.....The examiner must put aside knowledge of the applicant's disclosure, refrain from using hindsight, and consider the subject matter claimed 'as a whole.'"

Here, neither Pfiester nor Ahn teaches, or even suggests, the desirability of the combination since neither teaches or suggests forming three different spacer widths as recited in claim 5. Additionally, Pfiester discloses a gate structure comprising an oxide cap layer and nitride sidewall spacers. (See Pfiester, Fig. 6). However, Ahn discloses a gate structure, in the cell (memory) region, comprising a nitride cap layer and nitride sidewall spacers. (See Ahn, col. 3, lines 39-42; Figs.2a-2g). The nitride is important because it has a better selectivity than an oxide to secure an adequate process for contact etching for the bit line in the cell (memory) region. (See Ahn, col. 1, lines 12-15). Thus, it is clear that neither patent provides any incentive

or motivation supporting the desirability of the combination. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. § 103 rejection of claim 5.

In this context, the MPEP further provides at § 2143.01, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." The courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.

In the present case it is clear that the Examiner's combination arises solely from hindsight based on the invention without any showing, suggestion, incentive or motivation in either reference for the combination as applied to claim 5. Therefore, for this mutually exclusive reason, the examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

Claim 15

Claim 15 recites a transistor structure with three different spacer widths comprising "(c) oxide spacers having a width formed adjacent to said gate electrodes in said first, second, and third transistor regions; and (d) silicon nitride spacers having a first width formed on said oxide spacers in said first transistor region, silicon nitride spacers having a second width less than said first width formed on said oxide spacers in said second transistor region, and silicon nitride spacers having a third width less than said second width formed on said oxide spacers in said third transistor region." Claim 15 was rejected under 35 U.S.C. § 103 as being unpatentable over Pfiester in view of Ahn.

As stated in the Office Action, "it would have been obvious to a person having skill in the art to augment Pfiester's transistor structure...such as suggested by the combination of Pfiester's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer thicknesses, in order to form both CMOS transistors of both logic

and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance." Applicants respectfully traverse the assertion that it would have been obvious to augment Pfiester's transistor structure with the teachings of Ahn for at least some of the same reasons set forth above in claim 5.

Thus, the Examiner has not met his burden of supporting a *prima facie* case of obviousness and the rejection under 35 U.S.C. §103 should be withdrawn.

Claim 21

Claim 21 recites a transistor structure with three different spacer widths comprising "oxide spacers having a first width formed adjacent to said gate electrode in the first transistor region, oxide spacers having a second width that is less than said first width formed adjacent to said gate electrode in the second transistor region, and oxide spacers having a third width less than said second width formed adjacent to said gate electrode in the third transistor region." Claim 21 was rejected under 35 U.S.C. § 103 as being unpatentable over Pfiester in view of Ahn.

As stated in the Office Action, "it would have been obvious to a person having skill in the art to augment Pfiester's transistor structure...such as suggested by the combination of Pfiester's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer thicknesses, in order to form both CMOS transistors of both logic and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance." Applicants respectfully traverse the assertion that it would have been obvious to augment Pfiester's transistor structure with the teachings of Ahn for at least some of the same reasons set forth above in claim 5.

Thus, the Examiner has not met his burden of supporting a *prima facie* case of obviousness and the rejection under 35 U.S.C. §103 should be withdrawn.

Claims 18, 19, and 24

Claims 18, 19 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Pfiester in view of Ahn, as applied to claims 15 and 21, and further in view of Huang, et al. (US Patent No. 6,214,715 hereinafter referred to as "Huang"). Applicant traverses this rejection on the grounds that these references are defective in establishing a *prima facie* case of obviousness with respect to claims 18, 19 and 24.

Claims 18 and 19 depend from and further limit claim 15 and should be allowable for at least the same reasons as claim 15 set forth above.

Claim 24 depends from and further limits claim 21 and should be allowable for at least the same reasons as claim 21 set forth above.

Conclusion

It is clear from all of the foregoing that independent claims 5, 7, 10, 15, 16, 21 and 23 are in condition for allowance. Dependent claims 6, 8, 9,17-20, 22, 24 and 25 depend from and further limit independent claims 5, 7, 10, 15, 16 and 21 and therefore are allowable as well.

An early formal notice of allowance of claims 5-11 and 15-25 is requested. The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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